ABSTRACT OF THE DISCLOSURE

A digital adjustable chip oscillator comprising: a voltage control oscillator generating an oscillation signal, receiving a control voltage to adjust the frequency of the oscillation signal, and receiving an operating voltage to stabilize the frequency of the oscillation signal; a reference voltage circuit generating a reference voltage; a voltage regulation circuit receiving the reference voltage and generating the operating voltage; a digital tuning circuit receiving a digital code to adjust the control voltage and receiving the operating voltage to stabilize the control voltage; a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the frequency of the oscillation signal lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal; a programmable counter receiving a clock signal to trigger the counting and generating the digital code; a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high voltage comparison signal and directing the programmable counter to stop counting and hold the digital code; and a programmable memory receiving the enable signal to record the digital code.